Submission for 1999 electronic Pkg for Space Apps Workshop

Abstract

Testing and Qualification Lessons Learned Through the Direct Chip Attach/Mars Microprobe Team

It is a major goal of the tasks in the NASA Electronics Parts and Packaging Program (NEPP) to team with projects for the purpose of introducing new technologies and learn from the assembly and integration of flight hardware the problems associated with these technologies and their solutions. Chip on Board, MCM, and mixed technology assemblies were enabling for the DS2 mission but a new arena of test and development was entered. Questions such as how to probe during development tests, staged integration of bread board, brass board and flight hardware, environmental control and visibility into monolythic MCM assemblies are among those that had to be addressed. This presentation will address these questions, and others and the approaches utilized by DS2.

electronic packaging

Biography

Saverio D'Agostino graduated from The University of Illinois, Champaign/Urbana in 1970 with a B. S. in Metallurgical Engineering. Joined a Navy Materials Laboratory studying thin film structures and supporting the Navy's "captive" ASIC lines with process control and failure analysis. He left as Manager of the Engineering Materials Branch and joined the Materials Applications Group at JPL in 1979. He worked as Materials Engineer on Wide Field and Planetary Camera and the Galileo Spacecraft structure and RPM. As Technical Section Head of the Advanced Packaging Section at Hughes Missile Systems patented designs for stacked and high G (100,000 Gs) chip on board electronics. Returned to JPL in 1993 as packaging engineer on the MISR instrument and then Task Leader for Direct Chip Attachment in NASA's Advanced Interconnect Program. As Electronic Packaging Lead for the Mars Microprobe Project he teamed to develop COB electronics tightly integrated into its structure for high G survivability and volume efficiency.